FAIRCHILD SEMICONDUCTOR®

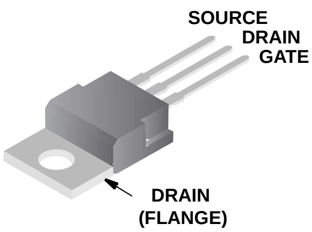
HUF76423P3, HUF76423S3S

Data Sheet | December 2001

33A, 60V, 0.035 Ohm, N-Channel, Logic Level UltraFET® Power MOSFET

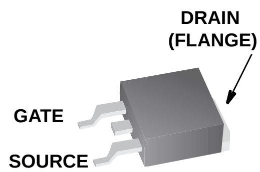
Packaging

JEDEC TO-220AB



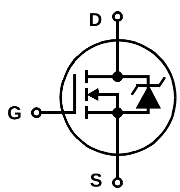
HUF76423P3

JEDEC TO-263AB



HUF76423S3S

Symbol



Features

- Ultra Low On-Resistance
  - $r_{DS(ON)} = 0.030\Omega$, $V_{GS} = 10V$
  - $r_{DS(ON)} = 0.035\Omega$, $V_{GS} = 5V$
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Electrical Models
  - Spice and SABER Thermal Impedance Models
  - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs R_{GS} Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF76423P3	TO-220AB	76423P
HUF76423S3S	TO-263AB	76423S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUF76423S3ST.

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HUF76423P3, HUF76423S3S	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	60	V
Gate to Source Voltage	V_{GS}	±16	V
Drain Current			
Continuous ($T_C = 25^oC$, $V_{GS} = 5V$)	I_D	33	A
Continuous ($T_C = 25^oC$, $V_{GS} = 10V$) (Figure 2)	I_D	35	A
Continuous ($T_C = 100^oC$, $V_{GS} = 5V$)	I_D	23	A
Continuous ($T_C = 100^oC$, $V_{GS} = 4.5V$) (Figure 2)	I_D	22	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	UIS	Figures 6, 17, 18	
Power Dissipation	P_D	85	W
Derate Above 25^oC		0.567	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief TB334	T_{pkg}	260	^oC

NOTES:

1. $T_J = 25^oC$ to 150^oC.

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Product reliability information can be found at http://www.fairchildsemi.com/products/discrete/reliability/index.html
For severe environments, see our Automotive HUFA series.
All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$ (Figure 12)		60	-	-	V
		$I_D = 250\mu A$, $V_{GS} = 0V$, $T_C = -40^oC$ (Figure 12)		55	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 55V$, $V_{GS} = 0V$		-	-	1	μA
		$V_{DS} = 50V$, $V_{GS} = 0V$, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 16V$		-	-	±100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$ (Figure 11)		1	-	3	V
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 35A$, $V_{GS} = 10V$ (Figures 9, 10)		-	0.025	0.030	Ω
		$I_D = 23A$, $V_{GS} = 5V$ (Figure 9)		-	0.029	0.035	Ω
		$I_D = 22A$, $V_{GS} = 4.5V$ (Figure 9)		-	0.032	0.038	Ω
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220 and TO-263		-	-	1.76	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	62	$^oC/W$
SWITCHING SPECIFICATIONS ($V_{GS} = 4.5V$)							
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 22A$ $V_{GS} = 4.5V$, $R_{GS} = 10\Omega$ (Figures 15, 21, 22)		-	-	245	ns
Turn-On Delay Time	$t_{d(ON)}$			-	12	-	ns
Rise Time	t_r			-	147	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	32	-	ns
Fall Time	t_f			-	50	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
SWITCHING SPECIFICATIONS ($V_{GS} = 10V$)							
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 35A$ $V_{GS} = 10V$, $R_{GS} = 10\Omega$ (Figures 16, 21, 22)		-	-	140	ns
Turn-On Delay Time	$t_{d(ON)}$			-	7	-	ns
Rise Time	t_r			-	85	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	47	-	ns
Fall Time	t_f			-	76	-	ns
Turn-Off Time	t_{OFF}			-	-	185	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 30V$, $I_D = 23A$, $I_{g(REF)} = 1.0mA$ (Figures 14, 19, 20)	-	28	34	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0V$ to $5V$		-	15	18	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0V$ to $1V$		-	1.2	1.5	nC
Gate to Source Gate Charge	Q_{gs}			-	3.5	-	nC
Gate to Drain “Miller” Charge	Q_{gd}			-	7	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz (Figure 13)		-	1060	-	pF
Output Capacitance	C_{OSS}			-	315	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	65	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 23A$	-	-	1.25	V
		$I_{SD} = 11.5A$	-	-	1.0	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 23A$, $dI_{SD}/dt = 100A/\mu s$	-	-	80	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 23A$, $dI_{SD}/dt = 100A/\mu s$	-	-	205	nC

Typical Performance Curves

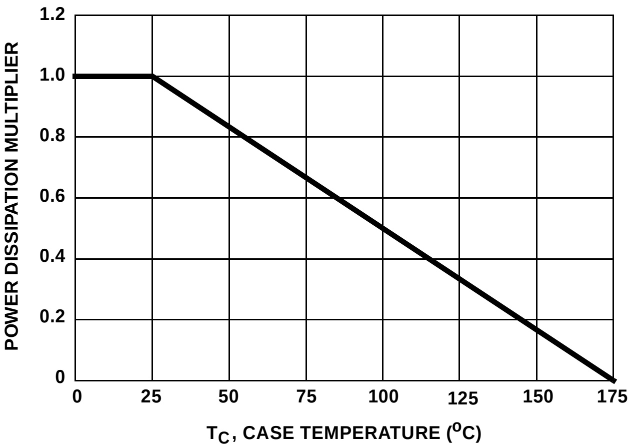


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

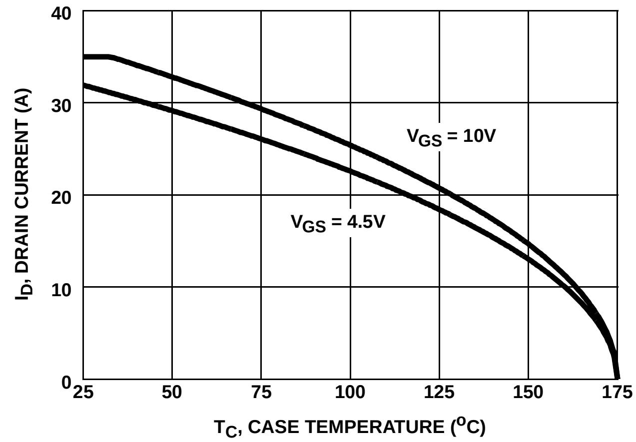


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

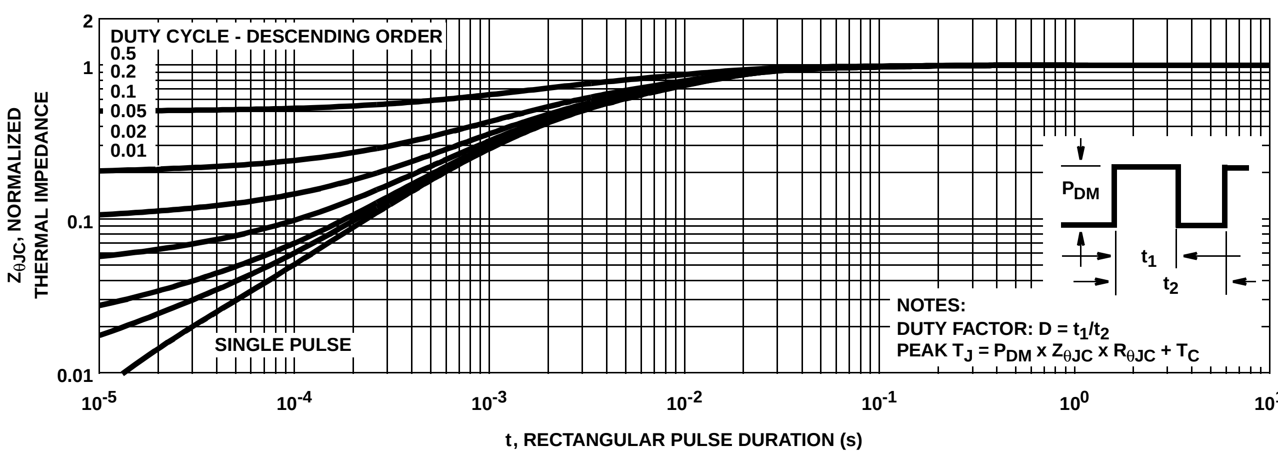


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

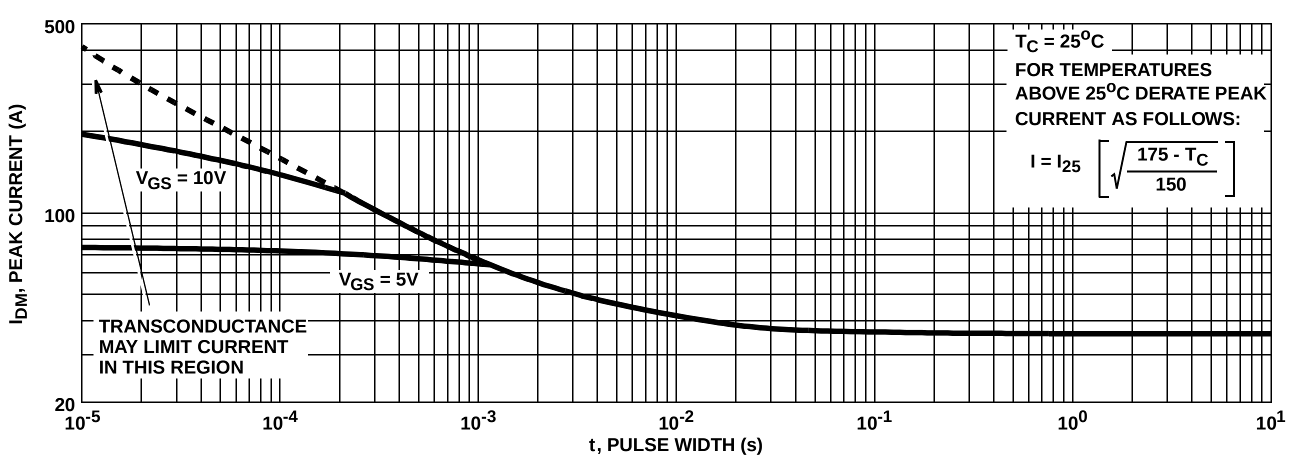


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

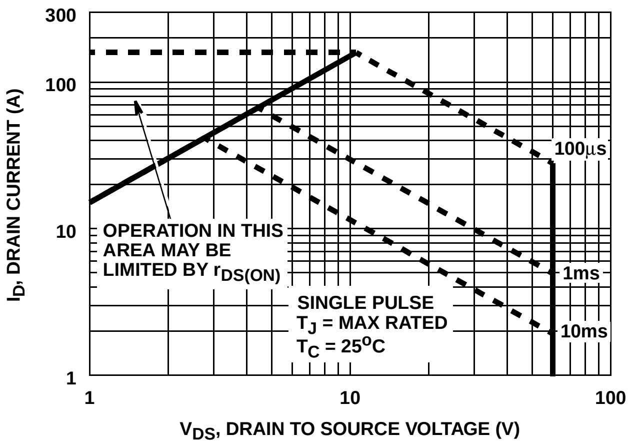
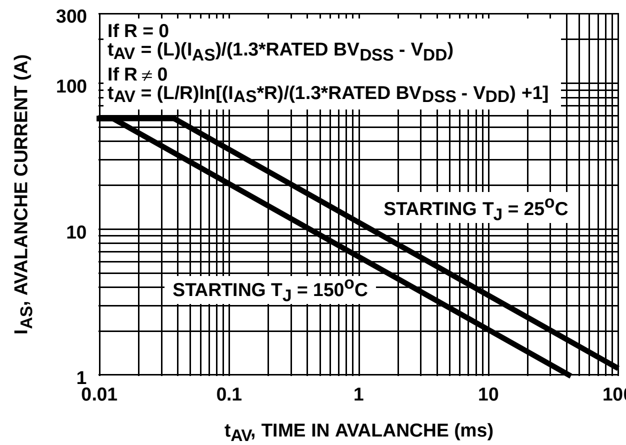


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

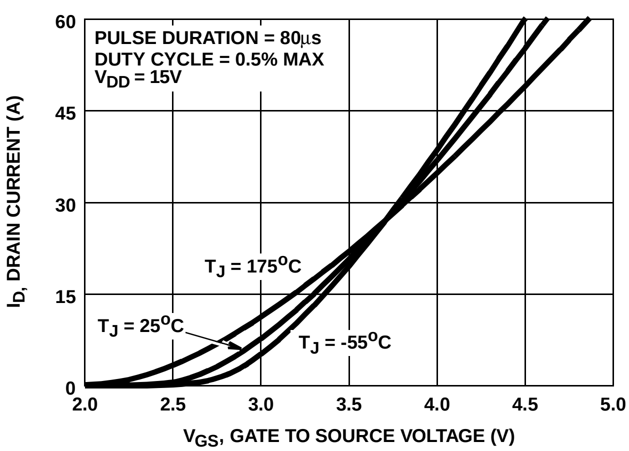


FIGURE 7. TRANSFER CHARACTERISTICS

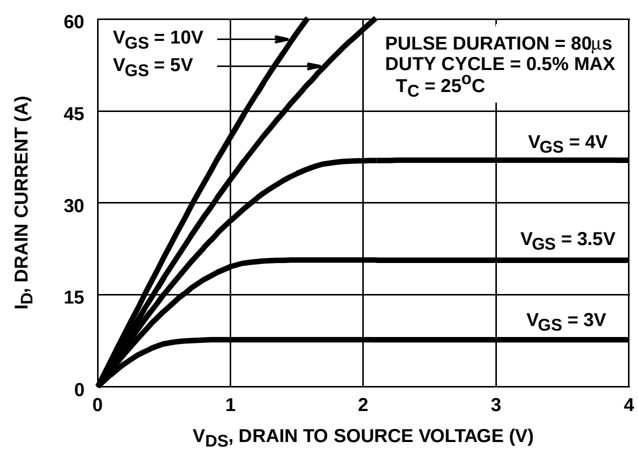


FIGURE 8. SATURATION CHARACTERISTICS

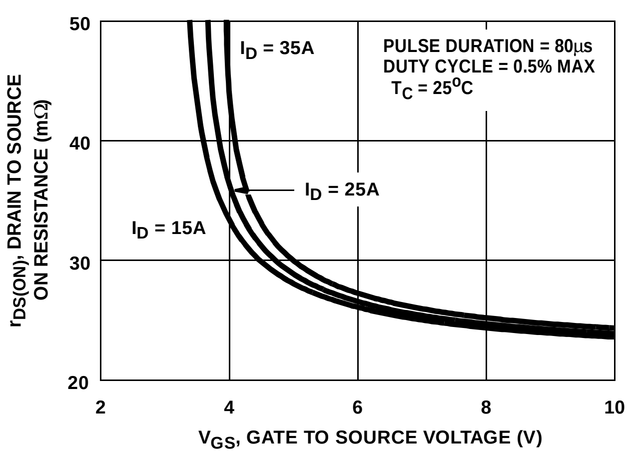


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

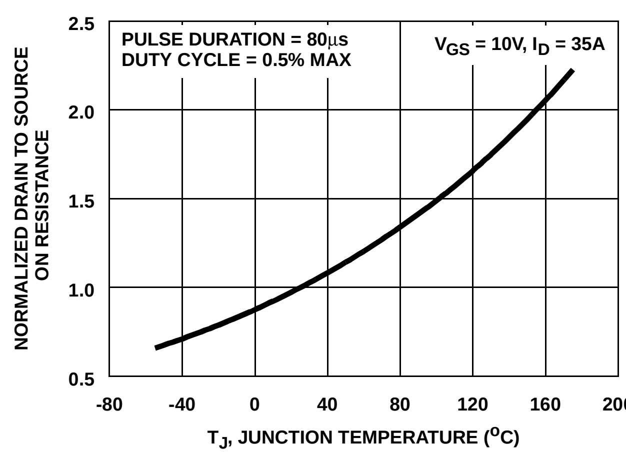


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

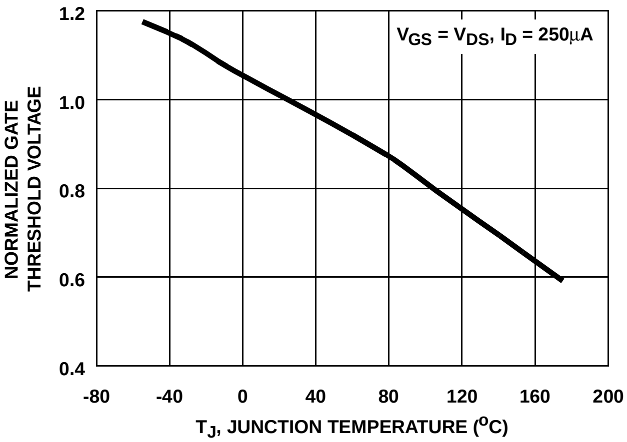


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

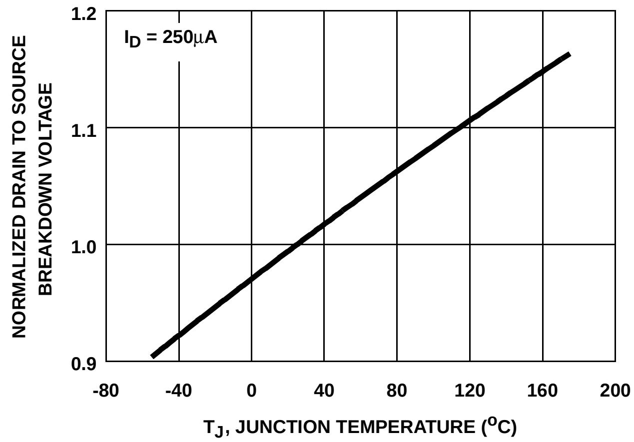


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

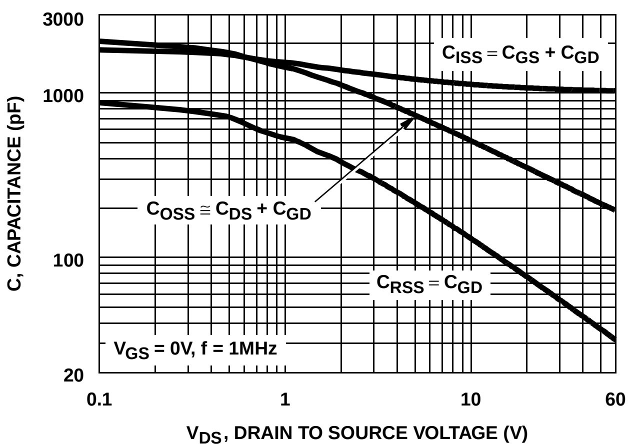
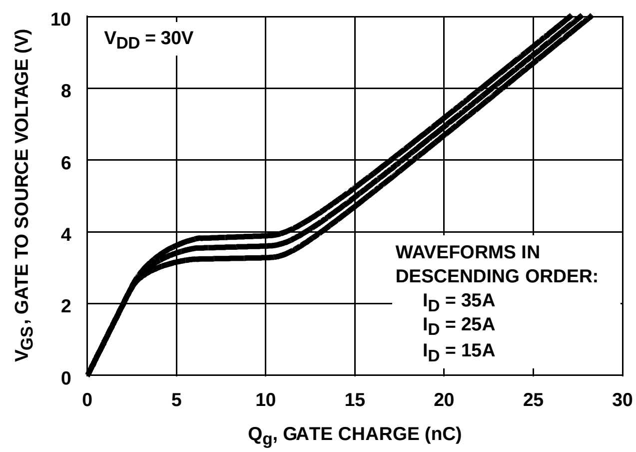


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

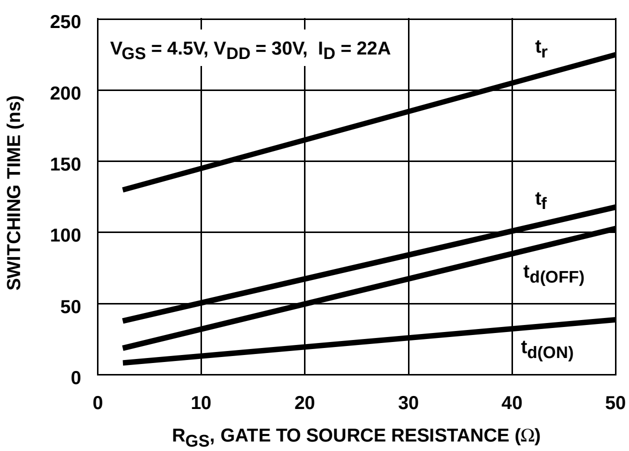


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

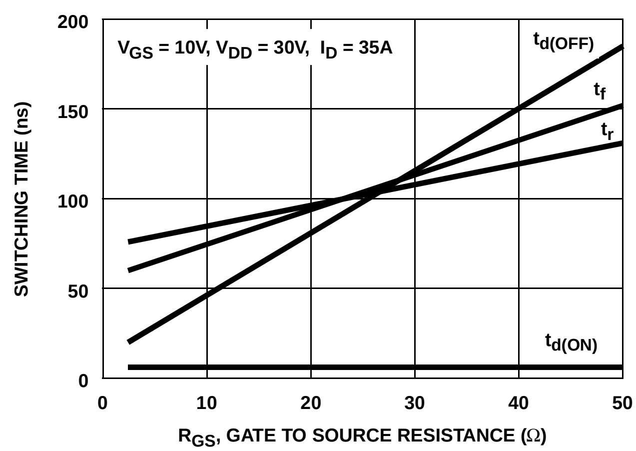


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

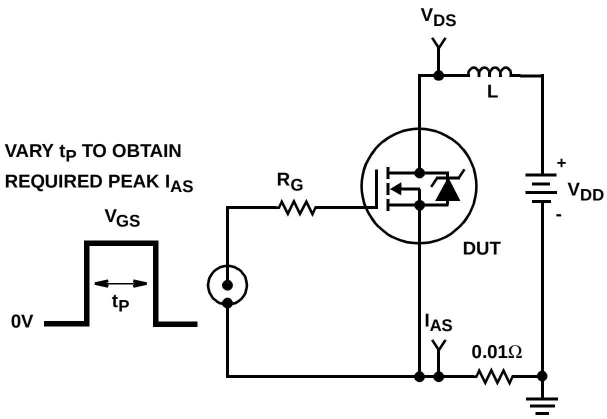


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

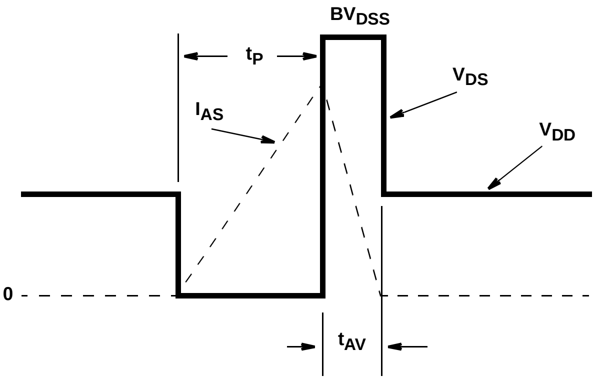


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

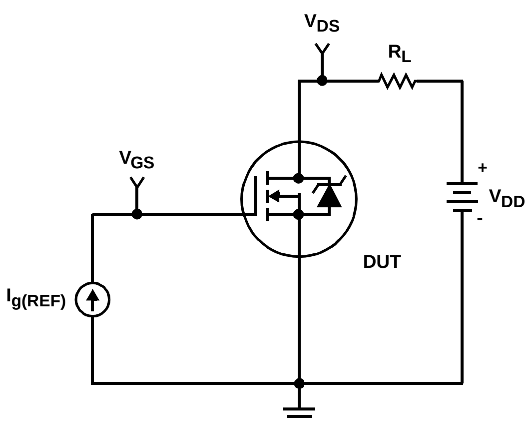


FIGURE 19. GATE CHARGE TEST CIRCUIT

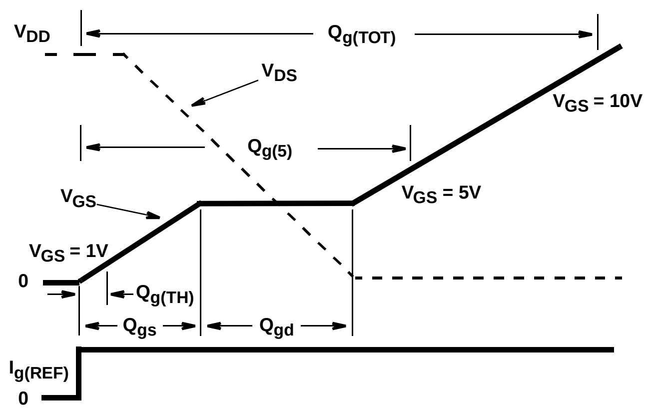


FIGURE 20. GATE CHARGE WAVEFORMS

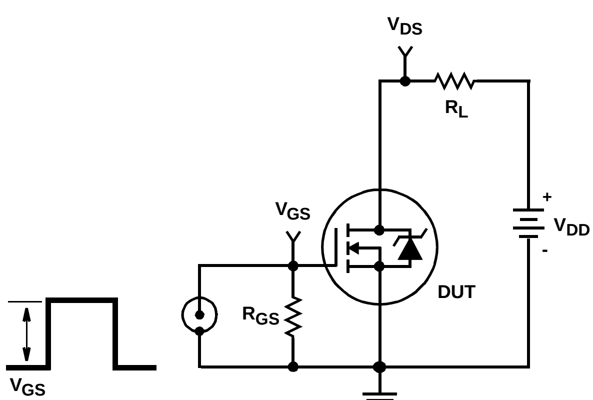


FIGURE 21. SWITCHING TIME TEST CIRCUIT

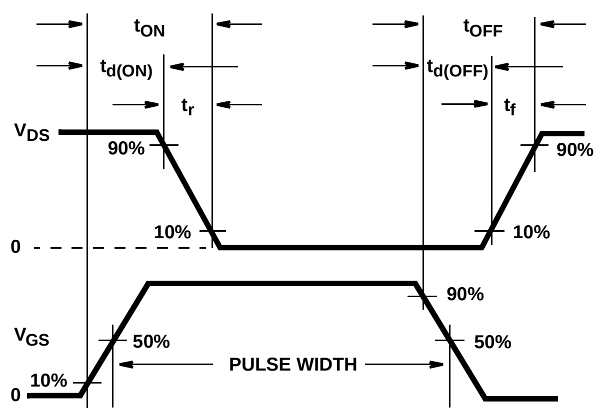


FIGURE 22. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

```
.SUBCKT HUF76423 2 1 3 ;     rev 7 September 1999

CA 12 8 1.46e-9
CB 15 14 1.46e-9
CIN 6 8 1.0e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 66.0
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

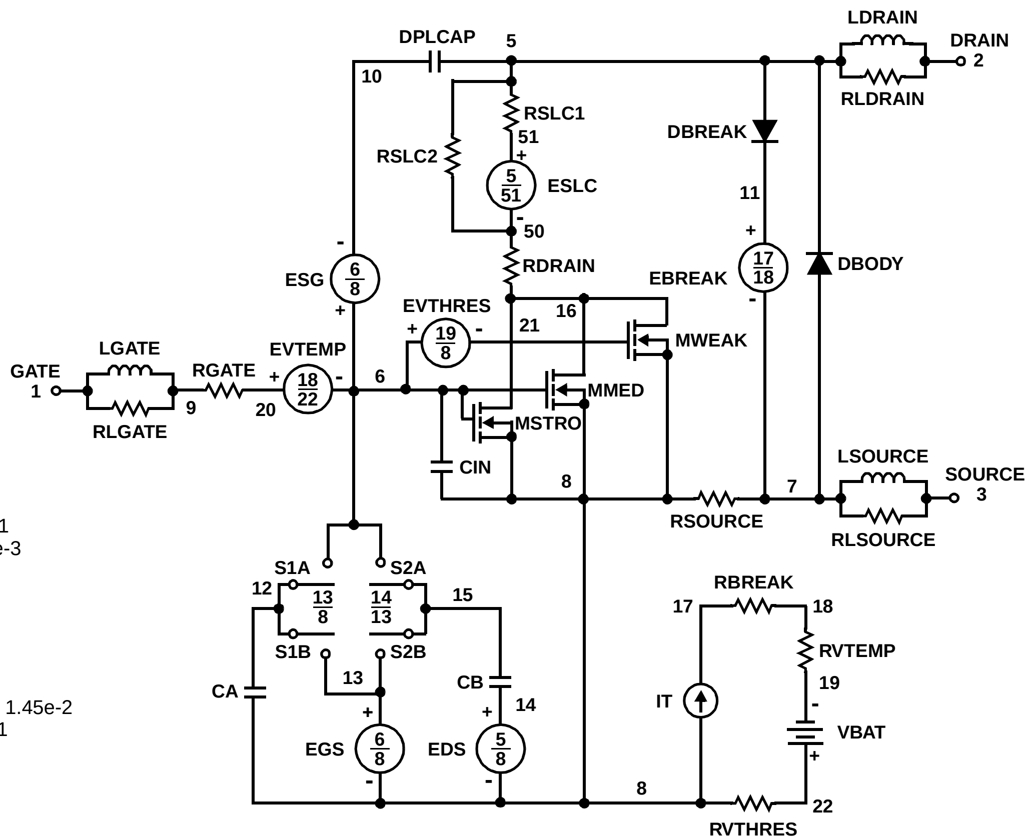
LDRAIN 2 5 1e-9
LGATE 1 9 5.5e-9
LSOURCE 3 7 4.4e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 7.0e-3
RGATE 9 20 3.6
RLDRAIN 2 5 10
RLGATE 1 9 55
RLSOURCE 3 7 44
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 1.45e-2
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1
```




```
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*100),3.5))}

.MODEL DBODYMOD D (IS = 6.3e-13 RS = 6.8e-3 TRS1 = 1e-3 TRS2 = 1e-6 XTI = 4.3 CJO = 1.28e-9 TT = 5.1e-8 M = 0.5)
.MODEL DBREAKMOD D (RS = 2.9e- 1TRS1 = 1e- 4TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 9.5e-1 0IS = 1e-3 0N = 10 M = 0.82)
.MODEL MMEDMOD NMOS (VTO = 2.10 KP = 6 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.6)
.MODEL MSTROMOD NMOS (VTO = 2.45 KP = 60.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.79 KP = 0.13 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 36 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.2e- 3TC2 = -5e-7)
.MODEL RDRAINMOD RES (TC1 = 1.3e-2 TC2 = 3.1e-5)
.MODEL RSLCMOD RES (TC1 = 5.5e-3 TC2 = 7e-6)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = -1.8e-3 TC2 = -5.8e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.7e- 3TC2 = 8e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.8 VOFF= -2.8)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.8 VOFF= -4.8)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.6 VOFF= 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF= -0.6)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV 7 September 1999

```
template huf76423 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
d..model dbodymod =  (is = 6.3e-13, xti = 4.3, cjo = 1.28e-9, tt = 5.1e-8, m = 0.50)
d..model dbreakmod = ()
d..model dplcapmod =  (cjo = 9.5e-10, is = 1e-30, n = 10, m = 0.82 )
m..model mmedmod = (type=_n, vto = 2.10, kp = 6, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.45, kp = 60.5, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.79, kp = 0.13, is = 1e-30, tox = 1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -4.8, voff = -2.8)
sw_vcsp..model s1bmod =  (ron =1e-5, roff = 0.1, von = -2.8, voff = -4.8)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -0.6, voff = 0.5)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 0.5, voff = -0.6)

c.ca n12 n8 = 1.46e-9
c.cb n15 n14 = 1.46e-9
c.cin n6 n8 = 1.0e-9

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1.0e-9
l.lgate n1 n9 = 5.5e-9
l.lsource n3 n7 = 4.4e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

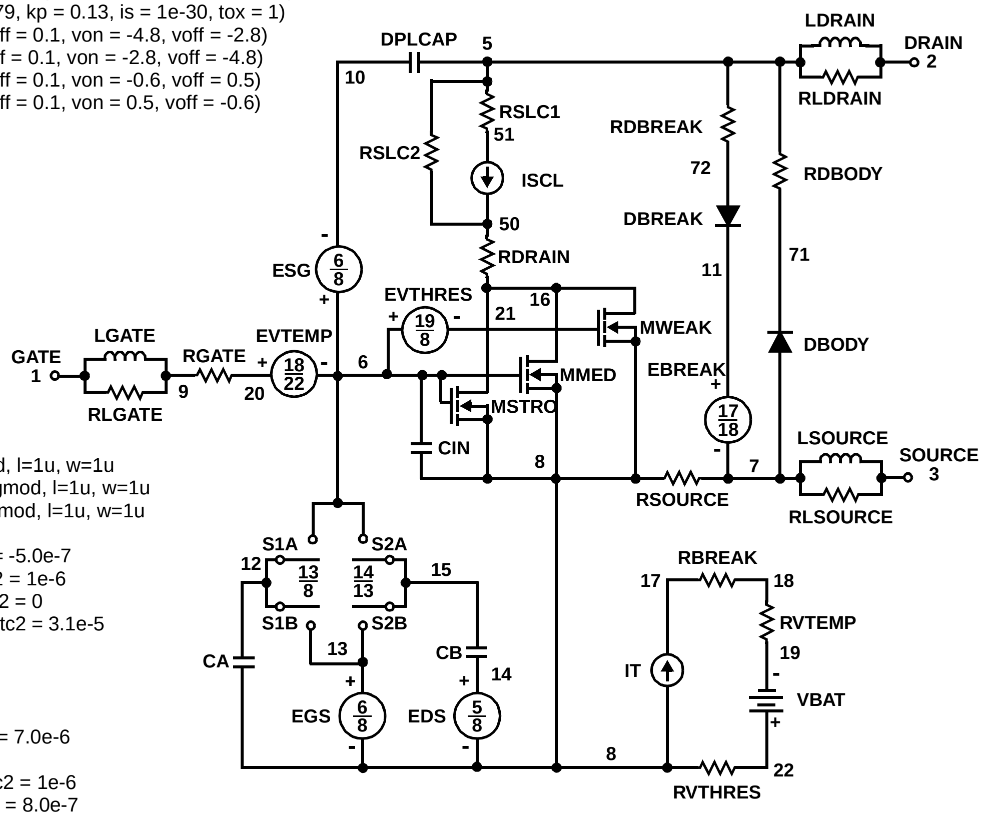
res.rbreak n17 n18  = 1, tc1 = 1.2e-3, tc2 = -5.0e-7
res.rdbody n71 n5 = 6.8e-3, tc1 = 1e-3, tc2 = 1e-6
res.rdbreak n72 n5 = 2.9e-1, tc1 = 1e-4, tc2 = 0
res.rdrain n50 n16  = 7.0e-3, tc1 = 1.3e-2, tc2 = 3.1e-5
res.rgate n9 n20 = 3.6
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 55
res.rlsource n3 n7 = 44
res.rslc1 n5 n51  = 1e-6, tc1 = 5.5e-3, tc2 = 7.0e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 1.45e-2, tc1 = 1e-3, tc2 = 1e-6
res.rvtemp n18 n19  = 1, tc1 = -1.7e-3, tc2 = 8.0e-7
res.rvthres n22 n8  = 1, tc1 = -1.8e-3, tc2 = -5.8e-6

spe.ebreak n11 n7 n17 n18 = 66.0
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/100))** 3.5))
}
}
```



SPICE Thermal Model

REV 1 September 1999

HUF76423T

CTHERM1 th 6 1.40e-3
CTHERM2 6 5 8.30e-3
CTHERM3 5 4 7.00e-3
CTHERM4 4 3 3.20e-3
CTHERM5 3 2 1.50e-2
CTHERM6 2 tl 1.10

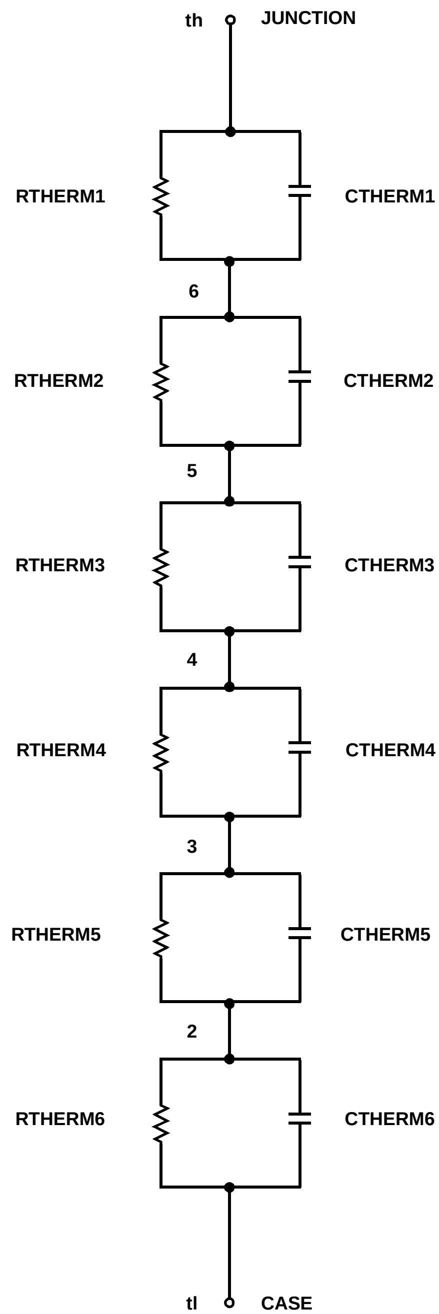
RTHERM1 th 6 1.20e-2
RTHERM2 6 5 2.99e-2
RTHERM3 5 4 8.43e-2
RTHERM4 4 3 4.73e-1
RTHERM5 3 2 7.14e-1
RTHERM6 2 tl 9.47e-2

SABER Thermal Model

SABER thermal model HUF76423T

template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 1.40e-3
ctherm.ctherm2 6 5 = 8.30e-3
ctherm.ctherm3 5 4 = 7.00e-3
ctherm.ctherm4 4 3 = 3.20e-3
ctherm.ctherm5 3 2 = 1.50e-2
ctherm.ctherm6 2 tl = 1.10

rtherm.rtherm1 th 6 = 1.20e-2
rtherm.rtherm2 6 5 = 2.99e-2
rtherm.rtherm3 5 4 = 8.43e-2
rtherm.rtherm4 4 3 = 4.73e-1
rtherm.rtherm5 3 2 = 7.14e-1
rtherm.rtherm6 2 tl = 9.47e-2
}



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